What is claimed is:

1. A semiconductor memory device comprising:

a memory that requires a refresh operation and has a predetermined number of divided memory spaces;

a register that stores information indicating whether the refresh operation is required or not with respect to each memory space;

an address counter that, with reference to the register, counts up an address while skipping an address for the memory space requiring no refresh operation to generate an address of the memory space to be refreshed; and

a cycle generating circuit that, with reference to the register, generates a refresh cycle of which cycle varies according to the number of the memory spaces requiring the refresh operation.

2. The semiconductor memory device according to claim 1, wherein the internal register can be reset from outside.

3. The semiconductor memory device according to claim 1, wherein the cycle generating circuit varies the refresh cycle so as to keep a cycle for refreshing the same

memory space constant regardless of the number of the memory spaces requiring the refresh operation.